# EAST Search History (Interference)

| Ref # | Hits | Search Query | DBs | Default Operator | Plurals | Time Stamp |
|---|---|---|---|---|---|---|
| L1 | 0 | (vertical semiconductor fin AND insulator layer AND doped source AND drain AND gate conductors).clm. | USPAT; UPAD | ADJ | OFF | 2009/11/04 10:15 |
| L2 | 0 | (vertical fin AND SOI substrate AND gate conductors AND sidewalls AND source conductors).clm. | USPAT; UPAD | ADJ | OFF | 2009/11/04 10:16 |
| L3 | 0 | (vertical semiconductor fin AND etching parallel trenches AND insulator layer AND depositing doped conductors).clm. | USPAT; UPAD | ADJ | OFF | 2009/11/04 10:16 |
| L4 | 0 | (vertical Fin-FET semiconductor device).clm. | USPAT; UPAD | ADJ | OFF | 2009/11/04 10:16 |
| S33 | 0 | "vertical semiconductor fin AND insulator layer AND doped source AND drain AND gate conductors".clm. | USPAT; UPAD | ADJ | OFF | 2009/11/03 13:18 |
| S34 | 0 | "vertical fin AND SOI substrate AND gate conductors AND sidewalls AND source conductors".clm. | USPAT; UPAD | ADJ | OFF | 2009/11/03 13:19 |
| S35 | 0 | "vertical semiconductor fin AND etching parallel trenches AND insulator layer AND depositing doped conductors".clm. | USPAT; UPAD | ADJ | OFF | 2009/11/03 13:19 |
| S36 | 0 | "vertical Fin-FET semiconductor device".clm. | USPAT; UPAD | ADJ | OFF | 2009/11/03 13:20 |